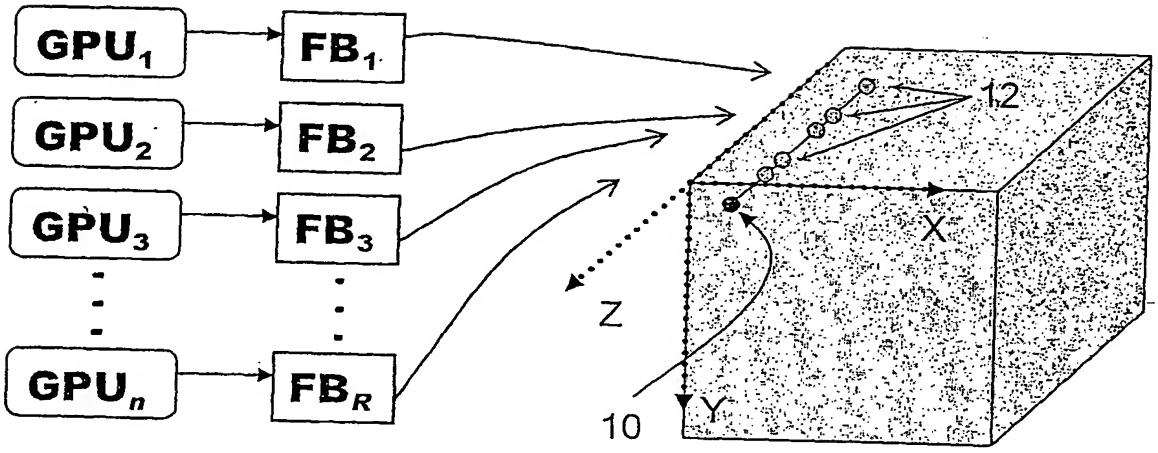


Fig. 1
(Prior Art)

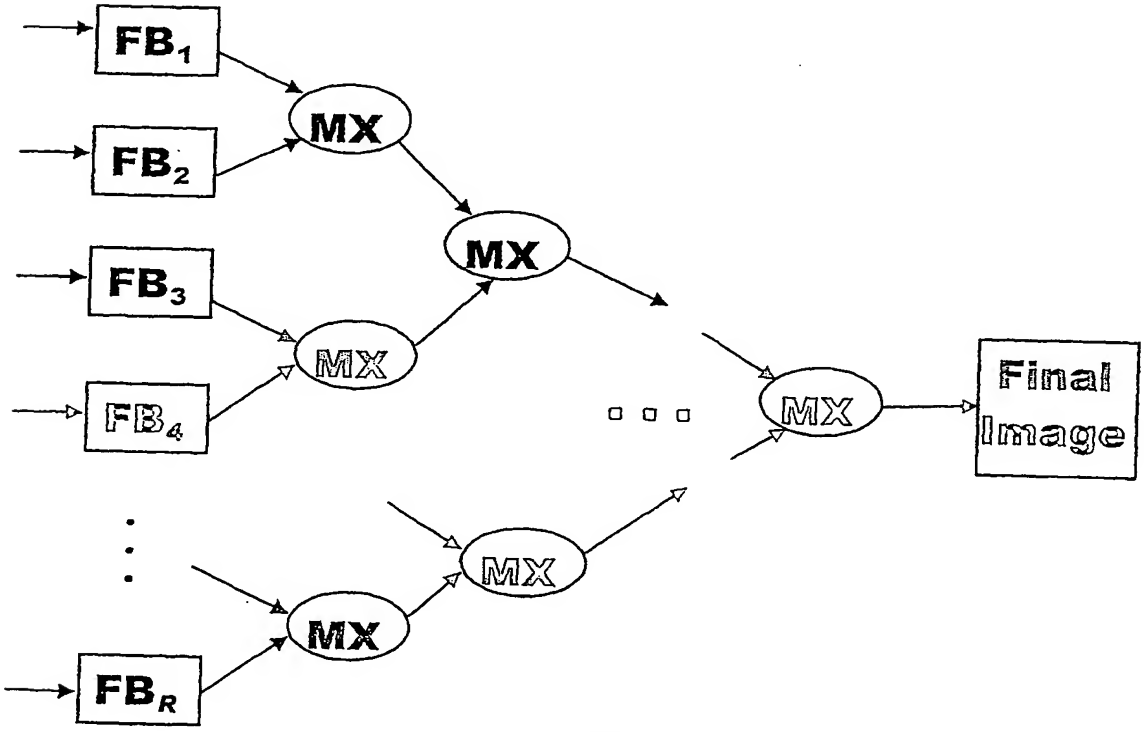


Fig. 2A
(Prior Art)

Fig. 2B (Prior Art)

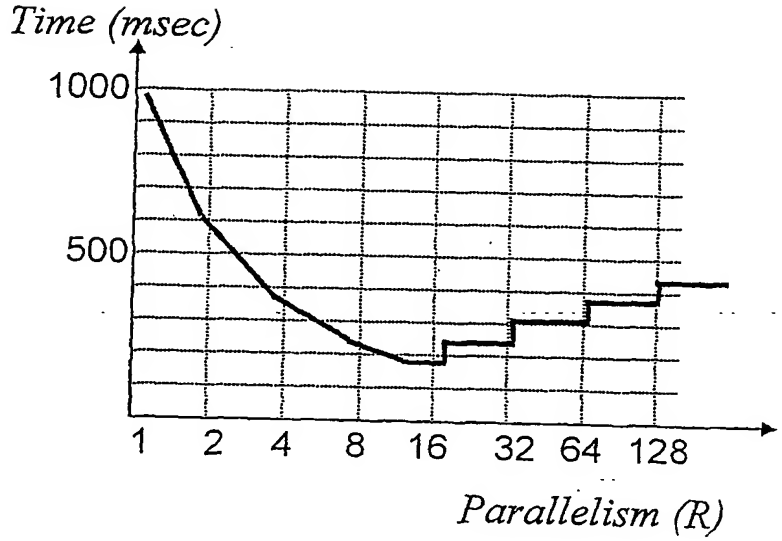
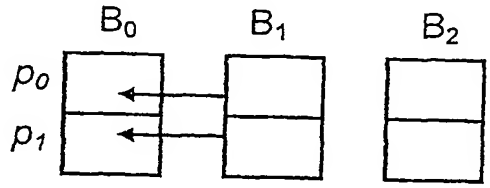


Fig. 3A (Prior Art)



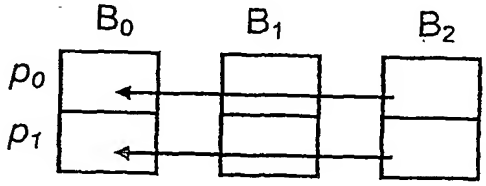


Fig. 3B (Prior Art)

Do in parallel

let B = sub-image i for processor p_i

for $n = 1, 2, 3, \ldots, P$

composite sub-images B_0 **and** B_n

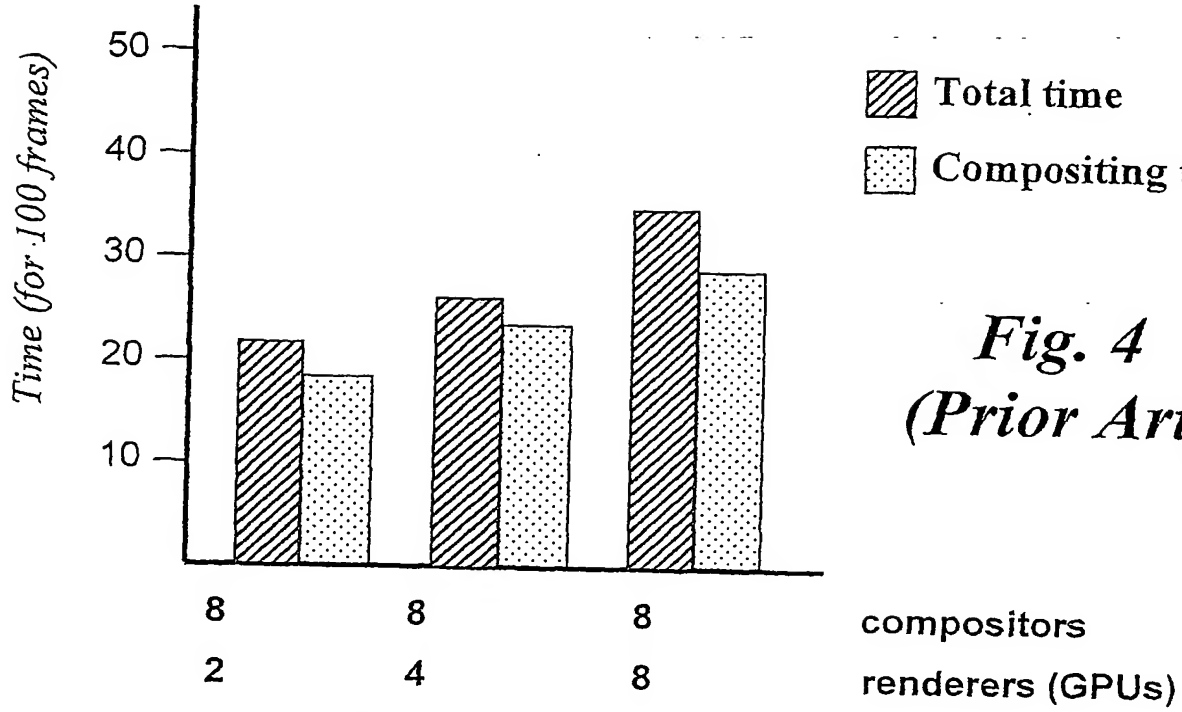


Fig. 4
(Prior Art)

Compositing time for 1024 images.

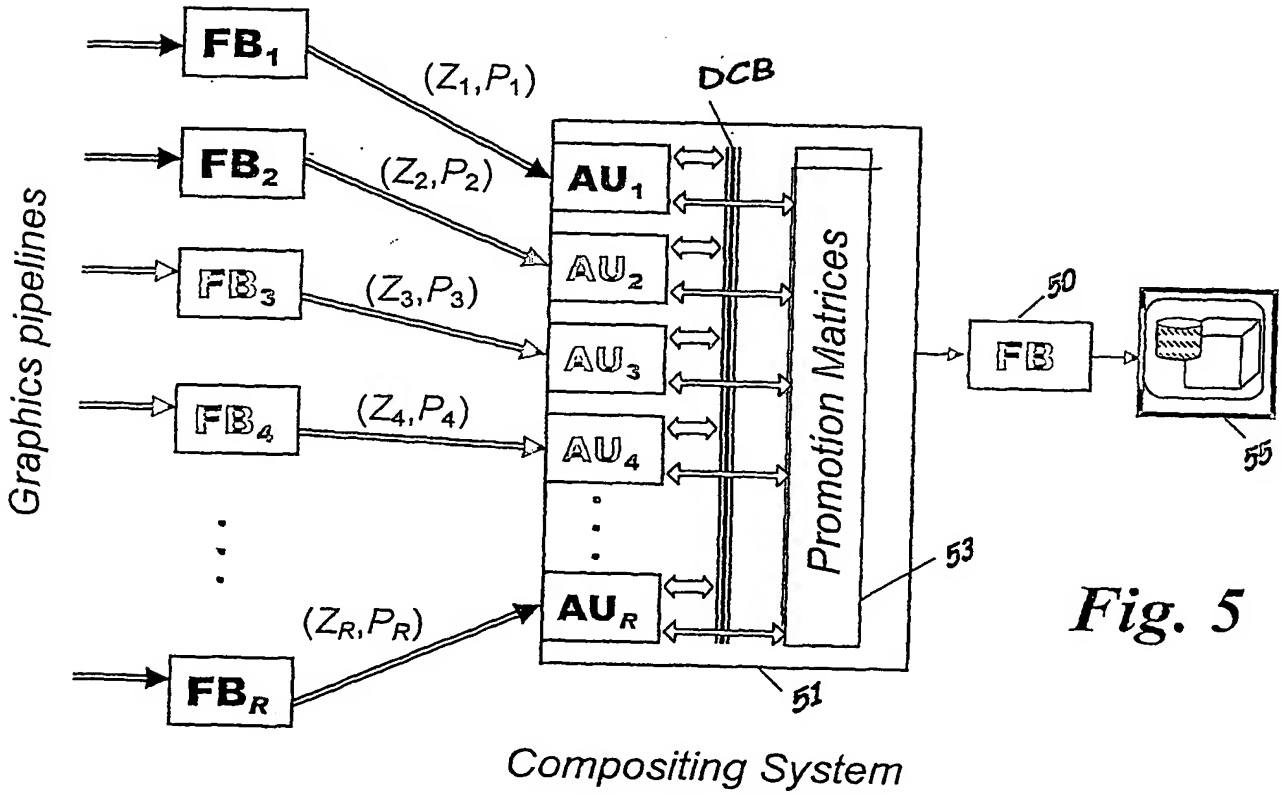


Fig. 5

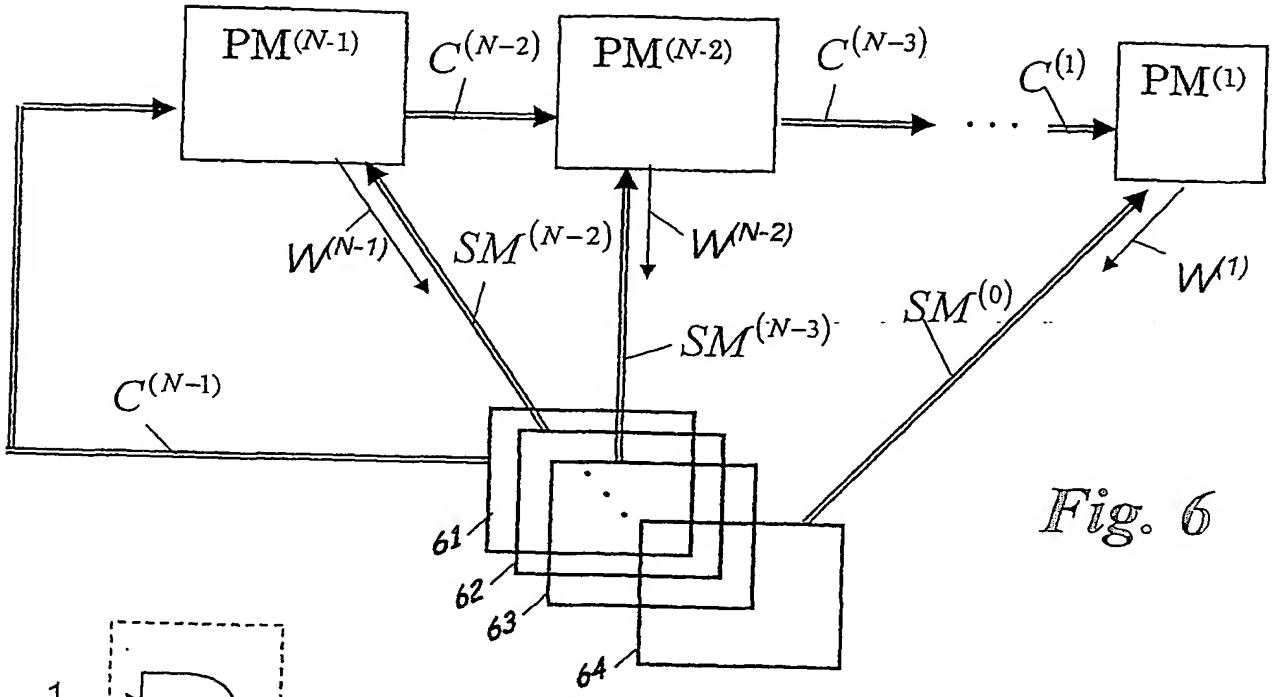


Fig. 6

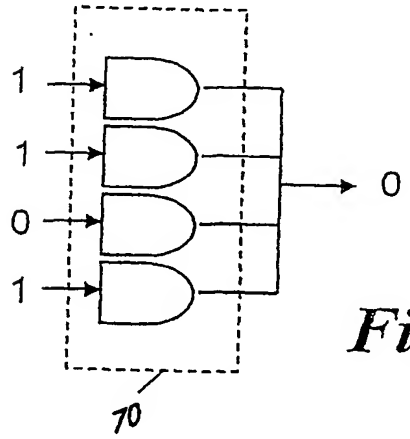


Fig. 7A

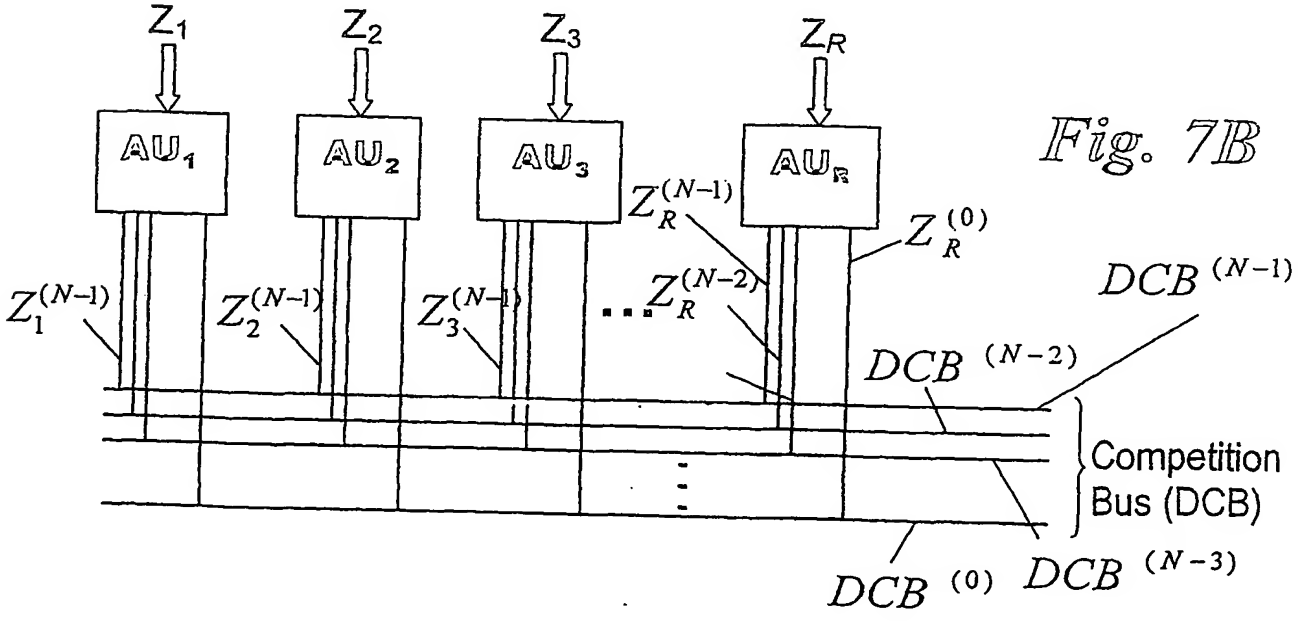


Fig. 7B

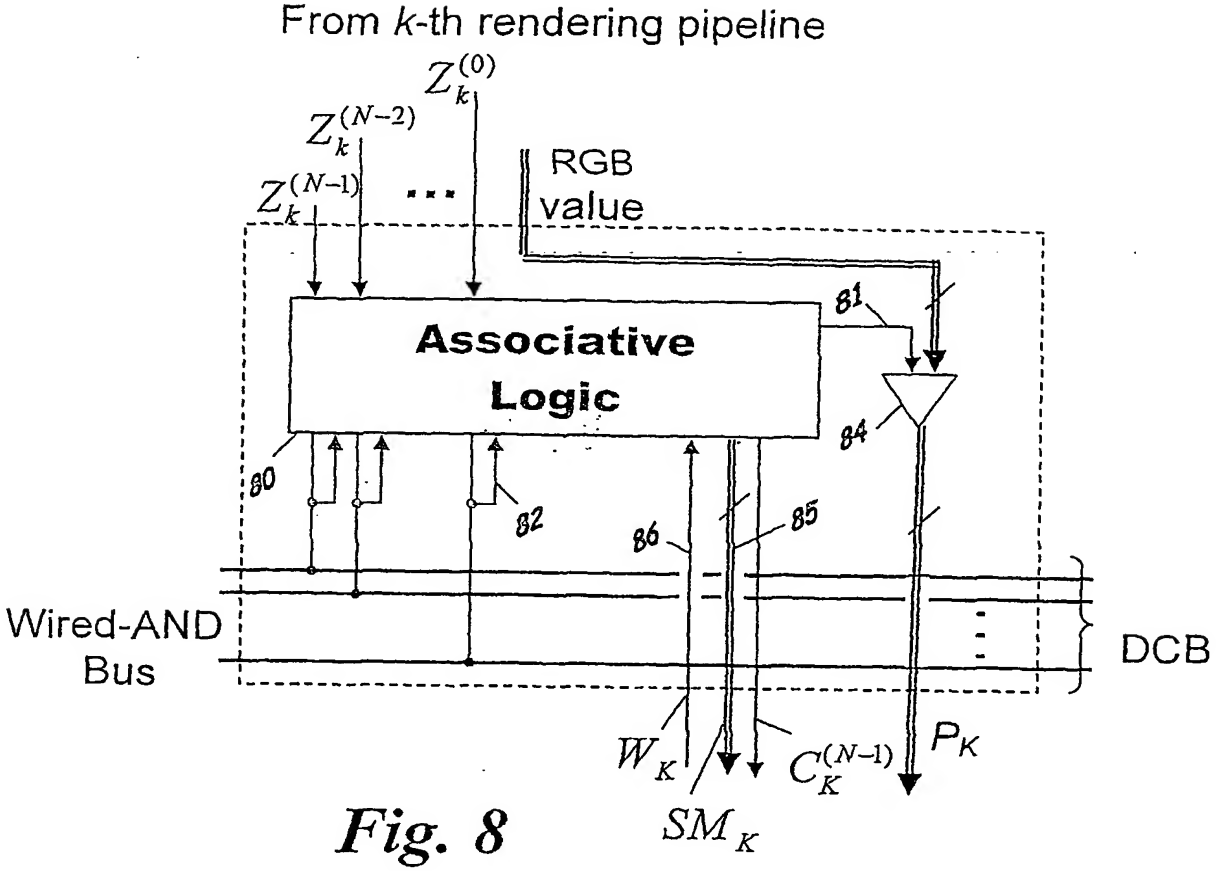

From k-th rendering pipeline
$Z_k^{(0)}$
$Z_k^{(N-2)}$
$Z_k^{(N-1)}$
RGB value
Associative Logic
81
84
80
82
86
85
Wired-AND Bus
DCB
W_K
SM_K
$C_K^{(N-1)}$
P_K

Fig. 8

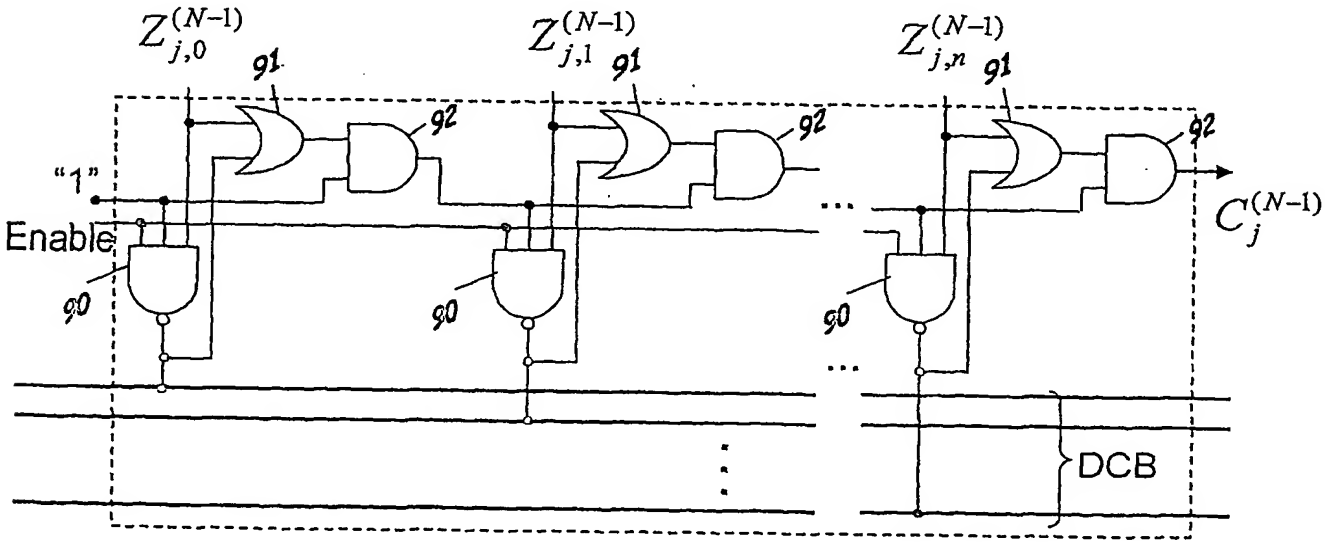

$Z_{j,0}^{(N-1)}$
$Z_{j,1}^{(N-1)}$
$Z_{j,n}^{(N-1)}$
91
92
"1"
Enable
90
DCB
$C_j^{(N-1)}$

Fig. 9

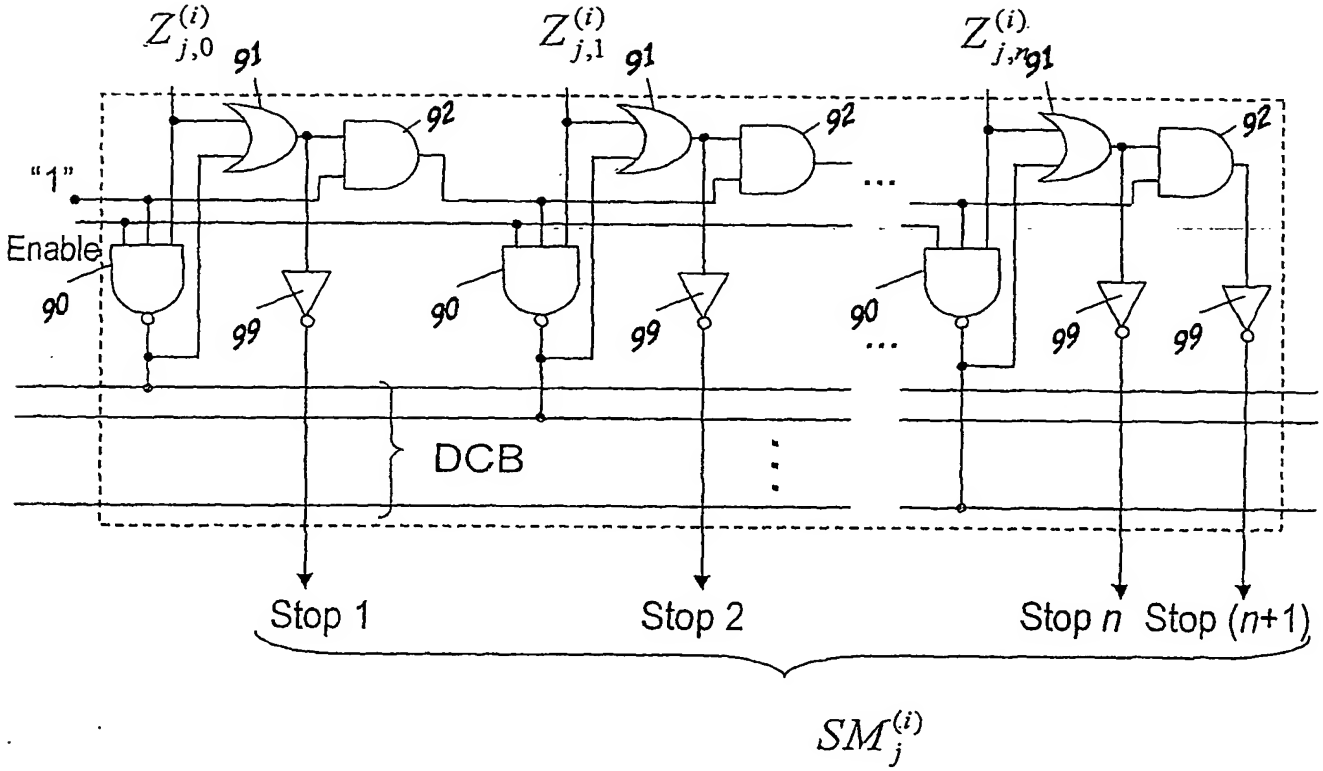
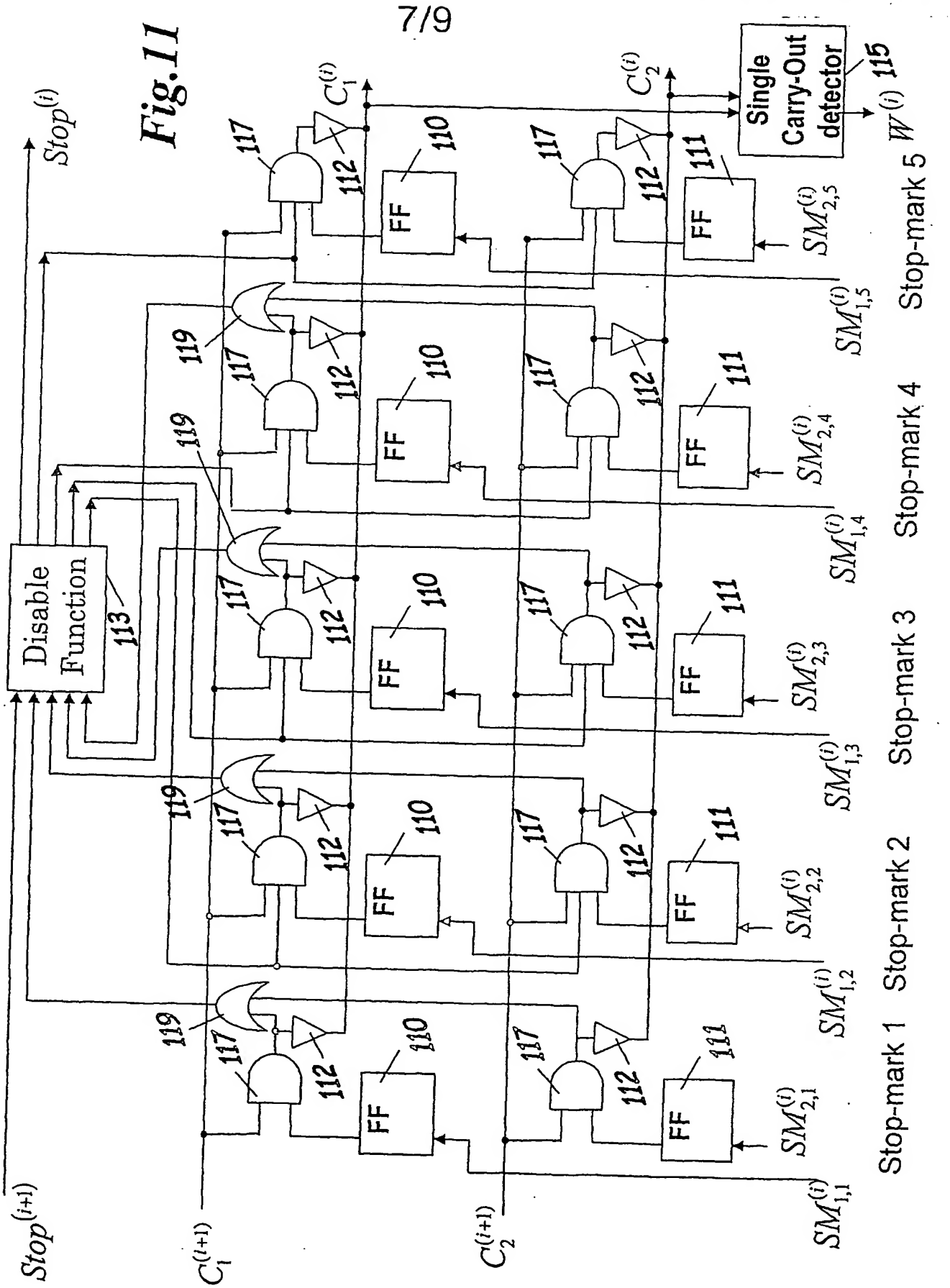

$Z_{j,0}^{(i)}$
$Z_{j,1}^{(i)}$
$Z_{j,n}^{(i)}$
91
92
"1"
Enable
90
99
DCB
Stop 1
Stop 2
Stop n
Stop (n+1)
$SM_j^{(i)}$

Fig. 10

Fig. 11



	Primary segment (8 bits) Carry-out(→) or stop	2nd segment (8 bits) Carry-in, stop-mark, carry-out	3d segment (8 bits) Carry-in, stop-mark, carry-out	4th segment (8 bits) Carry-in, stop-mark, carry-out	Win
a	stop	7	9		
b	→	→ 9 →	→ 9 →	→ 8 →	→
c	→	→ 8	9	7	
d	stop	9	9	7	
e	→	→ 9 →	→ 2	1	

Z_1:	10001001	10101000	01000011	11111111
Z_2:	10101010	10101011	01000011	11111110
Z_3:	10101010	10101010	01000011	11111101
Z_4:	10101000	10101011	01000011	11111100
Z_5:	10101010	10101011	00111111	00000000
	$Z_j^{(3)}$	$Z_j^{(2)}$	$Z_j^{(1)}$	$Z_j^{(0)}$

Fig. 12

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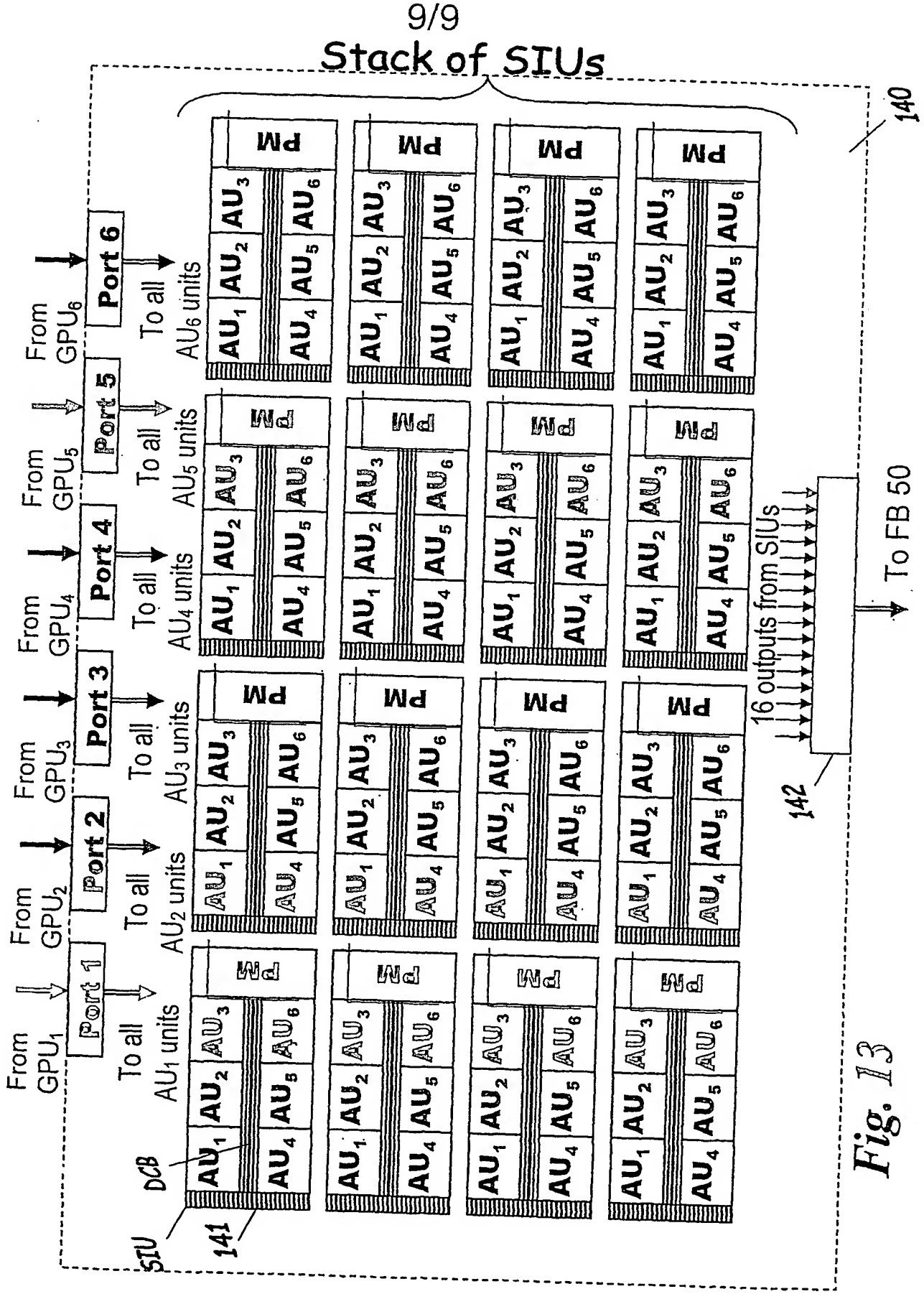
Stack of SIUs
140
From GPU1
From GPU2
From GPU3
From GPU4
From GPU5
From GPU6
Port 1
Port 2
Port 3
Port 4
Port 5
Port 6
To all AU1 units
To all AU2 units
To all AU3 units
To all AU4 units
To all AU5 units
To all AU6 units
AU1
AU2
AU3
AU4
AU5
AU6
PM
DCB
SIU
141
142
16 outputs from SIUs
To FB 50

Fig. 13